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DRN: COURSE.FDI0001

Author: Sadeque Reza Khan

Inverter Verilog Code:

```
module inv(a,b);
input a;
output b;
assign b=~a;
endmodule
```

Inverter Test Bench:

```
module inv_tb();
reg t_a;
wire t_b;
inv mygate(.a(t_a),.b(t_b));
initial
begin
$monitor (t_a,t_b);
t_a=1'b0;
#5 t_a =1'b1;
#5 t_a =1'b0;
#5 t_a =0'b1;
#5 t_a =0'b0;
end
endmodule
```